

Quantum Information Processing: Science & Technology

PI: Malcolm Carroll

Deputy PM: Tom Tarman

PM: Rebecca Horton

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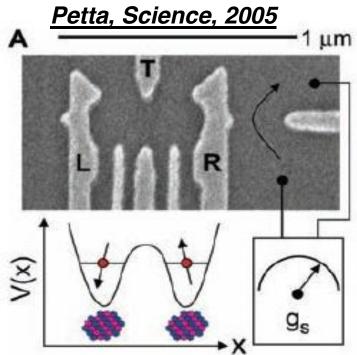
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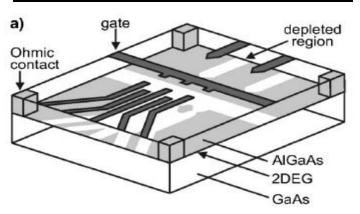


Solid-State Spin Qubit



- Qubits demonstrated using GaAs double quantum dots (DQD) [Petta, Science 2005]
- The qubit basis states are the (1) singlet and (2) triplet stationary states
- Long spin decoherence times in silicon spurs translation of GaAs qubit in to silicon

Hanson, Rev. Mod. Phys. 2007



Bloch Sphere (2 electron spins)

$$|1\rangle = |\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle$$

$$|\uparrow\downarrow\rangle$$

$$|0\rangle = |\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle$$



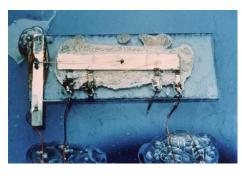




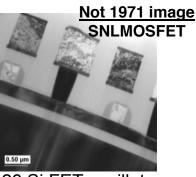
Ge BJT(1947)

Nobel Prize

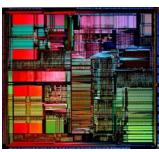
*MOSFET patent (1928)



First Integration in *Ge* (1959) *Nobel Prize**Integration in *Si* (1960)

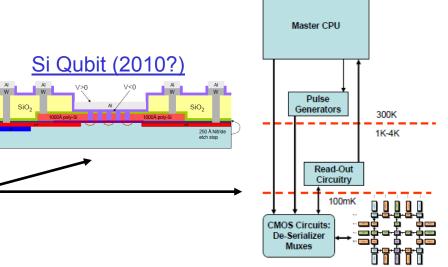


23 Si FET oscillator (1971)

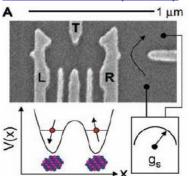


Modern CPU

Quantum Circuit (>2010)



GaAs Qubit (2005)



Marcus, Vienna, VA 2009

GaAs 2 Qubit Gate (2010?)

Quantum Information Science & Technology (QIST) Grand Challenge (3 years)

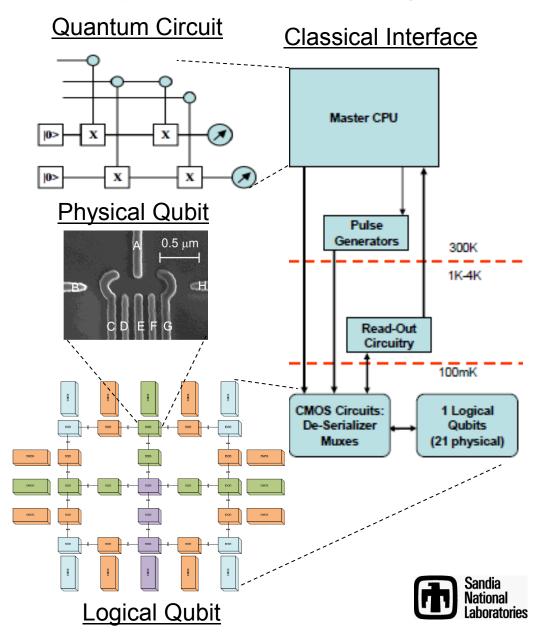
- 1. Demonstrate Si qubit (longer decoherence time)
- 2. Design error corrected logical qubit (quantum memory circuit)
 - Understand requirements for quantum circuit





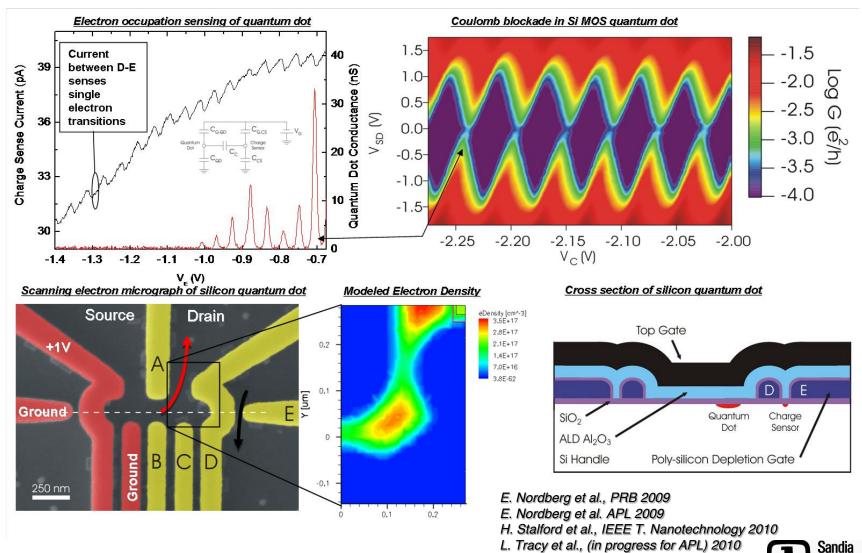
Multidisciplinary Grand Challenge

- Focus Areas
 - Physical Qubit (Si fab)
 - Electronics (Si CMOS)
 - Error Correction
 - Modeling
 - Second Generation Qubit





Single Charge Sensitive Sensor for Silicon Double Quantum Dot Qubit State Read-out



National

Laboratories

Single electron donor implants also under investigation



MOS DQD Qubit

Required steps

- Develop low disorder tunnel barriers point contacts
- 2. Develop low disorder stable quantum dots
- 3. Develop charge sensors (SET)

State-ofthe-art

- 4. Couple MOS QD and charge sensor
- 5. Develop few electron dots (w/ charge sensor)
- 6. Develop few electron DQD (w/ charge sensor)
- 7. T1 : Initialization and read-out of singlet vs. triplet (pulsed w/ charge sensing)
- 8. Integrate external dB for singlet/triplet evolution (if necessary?)
- 9. T2*: Rabi oscillations
- 10. T2: Hahn echo

SNL starts QIST Oct. 2007

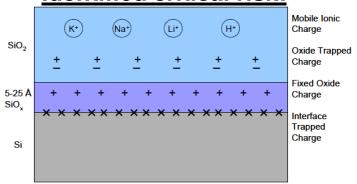
2006-7: NIST/NTT, CQCT & others

2008: CQCT **DQD 2008-10:** NTT, CQCT, **SNL**

2009: SNL, UCLA & others in 2010

2009-2010: UCLA, CQCT (donors)

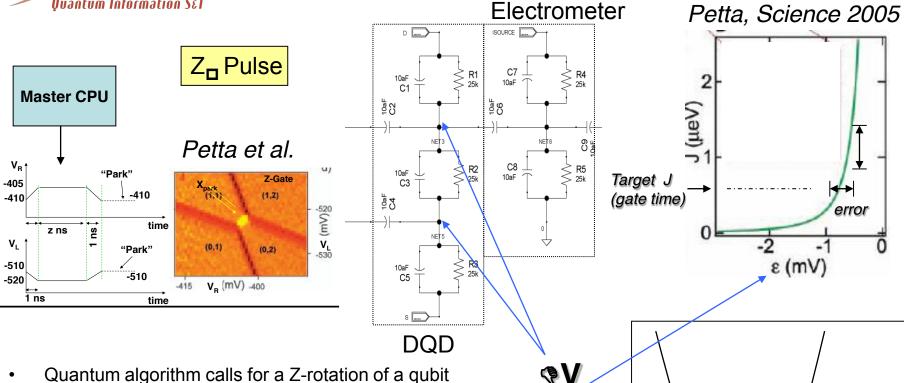
Identified critical risk:







"Circuit Designer Meets QIP"



- Accuracy & precision requirements produce clock constraints (3 ns not 120 ps)
 - Idle time is set relative to T2 (or T2*)
- Pulse shapes must be designed (will talk again about this later)
- Small signal model developed to bridge classical electronics and qubit physics
- Qubit design guidance is also suggested
 - Exchange flats [Nielsen et al. arXiv]



 $E_0 = \hbar \omega_0$

 $\approx -m\omega_0^2$

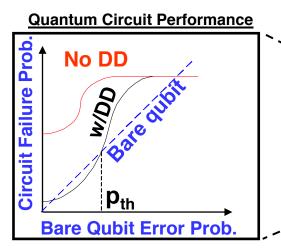
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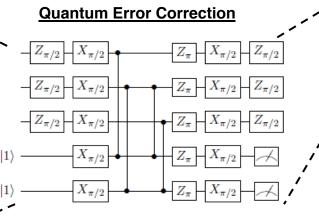
L

error



Logical Qubit Design in a Cryostat



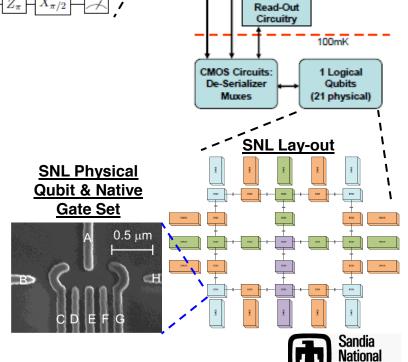


Goal: Can we design a beneficial error corrected memory (1st level) and for what range of T₂?

Approach:

- 1. Choose hardware defined by qubit
- 2. Choose quantum error correction
- 3. Optimize constrained schedule
- 4. Determine gate requirements for QEC circuit to provide benefit
- 5. improve & iterate (if necessary)

Result: $p_{threshold}$ BS9(21) = 4.7x10⁻⁴



SNL Classical Electronics Interface

Master CPU

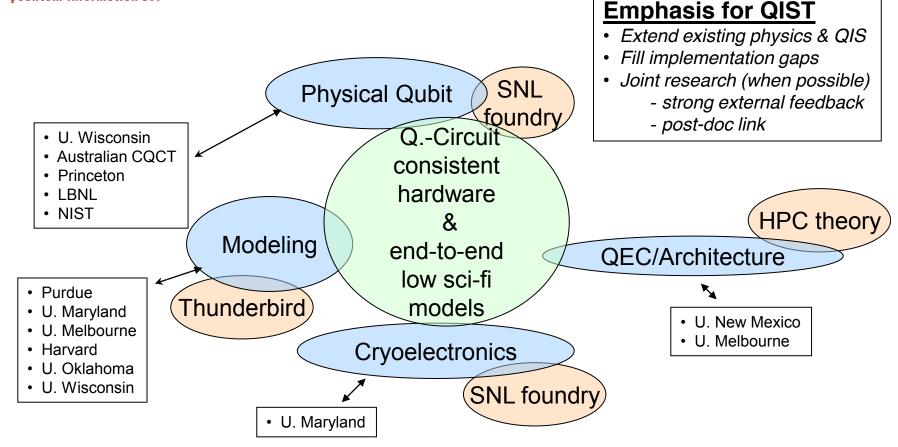
Pulse Generators

300K 1K-4K

Laboratories



Team, Resources & External Ties



The internal technical team

Physical qubit: M. Lilly, K. Childs, R. Grubbs, T. Lemp, J. Means, E. Nordberg*, B. Silva, J. Stevens, *G. Ten Eyck*, D. Tibbets, L. Tracy, J. Wendt, P. Hines, T. Pluym

2nd Generation: E. Bielejec, N. Bishop

Modeling: R. Muller, E. Nielsen, R. Rahman, H. Stalford**, W. Witzel, R. Young

Electronics: <u>T. Gurrieri</u>, <u>J. Levy</u>, J. Hamlet

Logical qubit: A. Landahl, R. Carr, A. Ganti, M. Grace, U. Onunkwo, C. Phillips, T. Tarman





Grand Challenge Summary

In the last 12 months:

21 invited talks

8 papers published

2 papers submitted

4 papers near submission

5 papers anticipated from recent results

GC Vision:

 Develop silicon qubit hardware and develop the capability to assess the scalability to a logical qubit built with the hardware

Magnitude & Impact

- Si DQDs offers an experimental platform to complement and advance current Si qubit technology
- Classical electronics, theory, and QEC combined with experimental model validation is producing a world-class logical qubit assessment
- Classical/quantum design experience and cryogenic CMOS is providing more general capability for QIP community
- GC project will produce a more integrated systems understanding of quantum circuitry at Sandia National Laboratories

Tools/Capabilities/Collaborations

- SNL has lab wide expertise to cover all critical areas (QIS is a big lab problem)
- Increased university & government lab collaboration being pursued



Moving Forward

Near term:

- Develop surface gate <u>enhancement mode</u> double quantum dots (MOS & strained-Si/SiGe) to:
 - Demonstrate few electrons & spin read-out
 - Examine impurity doped quantum-dots as an alternative architecture
- Use mobility, C-V, ESR, quantum dot performance & modeling to feedback and improve upon processing
 - Includes development of atomic precision fabrication at SNL
- Examine integrated electronics approaches to RF-SET
- Use combinations of numerical packages for multi-scale simulation of quantum dot systems (NEMO3D, EMT, TCAD, SPICE)
- Continue micro-architecture evaluation for different device and transport architectures

Long term:

- Experimental and modeling activities will continue under external funding
- Continuing strong interactions with universities and other national labs

QIST has established Sandia as a national and international resource in silicon quantum information science and technology.

